

United States Patent Application

For

STRUCTURE FOR SPANNING GAP IN BODY-BIAS VOLTAGE ROUTING
STRUCTURE

Inventors:

Robert P. Masleid

James B. Burr

Michael Pelham

Prepared by:

WAGNER, MURABITO & HAO LLP

Two North Market Street

Third Floor

San Jose, California 95113

(408) 938-9060

CONFIDENTIAL

STRUCTURE FOR SPANNING GAP IN BODY-BIAS VOLTAGE ROUTING STRUCTURE

5 BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention generally relates to semiconductor chips and MOSFETS (metal oxide semiconductor field effect transistors). More particularly, the present invention relates to the field of spanning gaps in the body-bias voltage routing

10 structure to the MOSFETS.

RELATED ART

Generation of the physical layout of a semiconductor device having MOSFETS (metal oxide semiconductor field effect transistors) formed on a semiconductor

15 substrate is a challenging task. An extensive amount of time and resources are spent during the creation of the physical layout. However, consumption of resources can be minimized if new physical layouts utilize substantial portions of existing physical layouts. For example, a new physical layout having MOSFETS that are body-biased would be less expensive to generate if an existing physical layout having MOSFETS
20 without body-bias is utilized and modified according to the needs of the new physical design. Unfortunately, this process of modifying the existing physical layout typically requires forming an additional routing layer for the body-bias voltage on the surface of the semiconductor device, creating a serious issue since the existing physical layout utilizes most, if not all, available surface area.

SUMMARY OF THE INVENTION

Embodiments of the present invention are directed to structures for spanning gap in body-bias voltage routing structure. In an embodiment, a structure is comprised of at least one metal wire.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the present invention.

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Figure 1 illustrates a top view of a pFET formed in an N-well in accordance with an embodiment of the present invention, showing the pFET having a body-bias voltage V_{nw} applied to its bulk/body B terminal.

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Figure 2A illustrates the relative positioning of an N-well and a deep N-well region beneath a surface of a semiconductor device in accordance with an embodiment of the present invention.

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Figure 2B illustrates a side view of a deep N-well region coupled to N-well_1 and N-well_2 in accordance with an embodiment of the present invention, showing the routing of the body-bias voltage.

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Figure 3A illustrates a top view of N-well_1 and N-well_2 in accordance with an embodiment of the present invention.

Figure 3B illustrates a top view of N-well_3 and N-well_4 in accordance with an embodiment of the present invention.

Figure 4 illustrates a top view of a semiconductor device in accordance with an embodiment of the present invention, showing multiple areas each area corresponding to a separate layout pattern for the deep N-well.

5 Figure 5A illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a diagonal sub-surface mesh structure in accordance with an embodiment of the present invention.

 Figure 5B illustrates a top view of multiple N-wells and multiple diagonal deep
10 N-well (DDNW) regions forming a diagonal sub-surface mesh structure in accordance with an embodiment of the present invention.

 Figure 6A illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a first diagonal sub-surface strip structure in accordance with an
15 embodiment of the present invention.

 Figure 6B illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a second diagonal sub-surface strip structure in accordance with an
embodiment of the present invention.

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 Figure 7 illustrates a top view of multiple axial deep N-well (ADNW) regions forming an axial sub-surface mesh structure in accordance with an embodiment of the present invention.

Figure 8A illustrates a top view of multiple axial deep N-well (ADNW) regions forming a first axial sub-surface strip structure in accordance with an embodiment of the present invention.

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Figure 8B illustrates a top view of multiple axial deep N-well (ADNW) regions forming a second axial sub-surface strip structure in accordance with an embodiment of the present invention.

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Figure 9A illustrates a top view of a semiconductor device, showing a first deep N-well mesh structure, a second deep N-well mesh structure, and an isolation structure formed between these deep N-well mesh structures to create a gap between these deep N-well mesh structures in accordance with an embodiment of the present invention.

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Figure 9B illustrates a top view of a semiconductor device, showing a deep N-well mesh structure and an isolation structure that creates a gap in the deep N-well mesh structure in accordance with an embodiment of the present invention.

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Figure 10 illustrates a cross-sectional view of the semiconductor device of Figure 9A along line A-B in accordance with an embodiment of the present invention.

Figure 11A illustrates a top view of semiconductor device of Figure 9A, showing a metal structure for spanning the isolation structure in accordance with an embodiment of the present invention.

- 5 Figure 11B illustrates a top view of semiconductor device of Figure 9B, showing a metal structure for spanning the isolation structure in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that

5 they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of

10 the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details.

Although the following description of the present invention will focus on routing

15 a body-bias voltage to pFETS (or p-type MOSFETS) formed in surface N-wells via a conductive sub-surface region of N-type doping when a p-type substrate and an N-well process are utilized, the present invention is equally applicable to routing a body-bias voltage to nFETS (or n-type MOSFETS) formed in surface P-wells via a conductive sub-surface region of P-type doping when an n-type substrate and a P-well

20 process are utilized.

LAYOUT PATTERNS FOR DEEP N-WELL REGION TO ROUTE BODY-BIAS VOLTAGE

Figure 1 illustrates a top view of a pFET 50 (or p-type MOSFET) formed in an N-well 10 when a p-type substrate and an N-well process are utilized in accordance with an embodiment of the present invention, wherein pFET 50 has a body-bias voltage V_{nw} applied to its bulk/body B terminal. As depicted in Figure 1, pFET 50 has gate G, drain D (p-type doping), source S (p-type doping), and bulk/body B terminals. In particular, bulk/body B terminal is coupled to N-well 10. Hence, a voltage applied to bulk/body B terminal is received by N-well 10. The N-well has an n-type doping. Regions of a semiconductor device that are doped with an n-type dopant have one type of conductivity while regions that are doped with a p-type dopant have another type of conductivity. Typically, various dopant concentrations are utilized in different regions of the semiconductor device.

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The pFET 50 is body-biased to influence its performance. Without body-biasing, the source S and bulk/body B terminals may be coupled together. With body-biasing, the source S and bulk/body B terminals are not coupled together. Body-biasing enables controlling the potential difference between the source S and bulk/body B terminals of the pFET 50, providing the ability to electrically tune the threshold voltage level of the pFET 50.

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In the case of body-biasing, bulk/body B terminal receives a body-bias voltage V_{nw} . As described above, bulk/body B terminal represents a connection to N-well 10. Thus, the body-bias voltage V_{nw} is applied to N-well 10.

5 Instead of generating an entire new physical layout for a semiconductor device to support pFET 50 having the body-bias voltage V_{nw} , an existing physical layout can be modified. In particular, the existing physical layout is modified by including a deep N-well region to route the body-bias voltage V_{nw} to N-wells 10 which generally are separated by P-well regions, wherein deep N-well represents a conductive sub-
10 surface well layer that is beneath the surface N-well 10. This avoids having to create another surface routing layer on a surface of the semiconductor device that does not have much free surface area for additional routing.

Several layout patterns for the deep N-well region are described herein. These
15 layout patterns facilitate routing the body-bias voltage in the semiconductor device. The layout patterns include a diagonal sub-surface mesh structure (see Figure 5A), an axial sub-surface mesh structure (see Figure 7), a diagonal sub-surface strip structure (see Figure 6A and Figure 6B), and an axial sub-surface strip structure (see Figure 8A and Figure 8B). A particular layout pattern is selected for an area of the semiconductor
20 device according to several factors as will be described below. Once the particular layout pattern is selected, the layout for the deep N-well region can be generated in an automated manner.

The body-bias voltage V_{nw} is routed to the N-wells via one or more deep N-well regions (which are conductive sub-surface well layers) as opposed to surface metal layers. In one embodiment, the deep N-well region is a diagonal deep N-well region as will be described below. In another embodiment, the deep N-well region is an axial
5 deep N-well region as will be described below. The advantage of this approach is that while typically there is little or no room on the densely packed surface area of the semiconductor device for extra metal routing layers, the area beneath the surface of the semiconductor device is often underutilized due to the fact that routing signals through wells is generally prohibited by the poor frequency response and potentially
10 unfavorable resistance of the wells. In the present invention, rather than carrying signals, the deep N-well regions serve to hold and distribute the body-bias voltage V_{nw} .

Figure 2A illustrates the relative positioning of an N-well 10 (also known as a
15 surface N-well) and a deep N-well region 20 beneath a surface 70 of a semiconductor device in accordance with an embodiment of the present invention. N-well 10 is formed beneath surface 70 of the semiconductor device and has an N-type doping. Deep N-well region 20 is formed beneath N-well 10 such that deep N-well region 20 and N-well 10 share a sub-surface conductive boundary 25 that allows deep N-well
20 region 20 to function like a conductive sub-surface routing layer for routing the body-bias voltage V_{nw} to the N-wells. That is, deep N-well region 20 contacts N-well 10 along the sub-surface conductive boundary 25. Moreover, deep N-well region 20 is buried under surface 70 of the semiconductor device. Deep N-well region 20 has an

N-type doping. It should be understood that if an n-type substrate and a P-well process were utilized, a deep well of P-type doping would be utilized to function as a conductive sub-surface routing layer for routing the body-bias voltage to the surface P-wells.

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The dimensions and size of the sub-surface conductive boundary 25 determine the resistance of the conductive path between N-well 10 and deep N-well region 20. As the size of sub-surface conductive boundary 25 is increased, the resistance of sub-surface conductive path between N-well 10 and deep N-well region 20 is lowered to
10 create a low-resistance conductive path.

Figure 2B illustrates a side view of a deep N-well region coupled to N-well_1 and N-well_2 in accordance with an embodiment of the present invention, showing the routing of the body-bias voltage. As illustrated in Figure 2B, there is a first sub-surface
15 conductive boundary 396 between N-well_1 and deep N-well region 310. Moreover, there is a second sub-surface conductive boundary 397 between N-well_2 and deep N-well region 310. Surface N-well_1 has a PFET 370. Also, surface N-well_2 has a PFET 370. The P-well region has an NFET 380 and separates N-well_1 and N-well_2. The body-bias voltage V_{nw} is routed to N-well_1 and N-well_2 via the first
20 and second sub-surface conductive boundaries 396 and 397.

A top view of N-well_1 and N-well_2 in accordance with an embodiment of the present invention is illustrated in Figure 3A. As depicted in Figure 3A, N-well_1 and N-

well_2 have an axial orientation. That is, N-well_1 and N-well_2 are positioned along an axis (e.g., x-axis). N-well_1 and N-well_2 have an N-type doping. The body-bias voltage V_{nw} is routed to N-well_1 and N-well_2 so that pFETs 370 can be body-biased via the deep N-well region. Thus, a contact for the body-bias voltage V_{nw} can be formed wherever there is free surface area, such as above N-well_1, N-well_2, or deep N-well region. Since N-well_1 and N-well_2 are separated by a P-type region or P-well region 385 on which nFETS 380 are formed, the layout pattern of the deep N-well is carefully selected to avoid isolating the P-type region or P-well region 385 on which nFETS 380 are formed, allowing the formation of conductive paths between P-well region 385 and a sub-surface layer (e.g., doped with P-type material) that is formed beneath the deep N-well region. Here, N-well_1 and N-well_2 are separated by the length d .

Figure 3B illustrates a top view of N-well_3 and N-well_4 in accordance with an embodiment of the present invention. As depicted in Figure 3B, N-well_3 and N-well_4 also have an axial orientation. That is, N-well_3 and N-well_4 are positioned along an axis (e.g., y-axis). N-well_3 and N-well_4 have an N-type doping. The body-bias voltage V_{nw} is routed to N-well_3 and N-well_4 so that pFETs 370 can be body-biased via the deep N-well region. Thus, a contact for the body-bias voltage V_{nw} can be formed wherever there is free surface area, such as above N-well_3, N-well_4, or deep N-well region. Since N-well_3 and N-well_4 are separated by a P-type region or P-well region 385 on which nFETS 380 are formed, the layout pattern of the deep N-well is carefully selected to avoid isolating the P-type region or P-well region 385 on

which nFETS 380 are formed, allowing the formation of conductive paths between P-well region 385 and a sub-surface layer (e.g., doped with P-type material) that is formed beneath the deep N-well region. Here, N-well_3 and N-well_4 are separated by the length m.

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Figure 4 illustrates a top view of a semiconductor device 400 in accordance with an embodiment of the present invention, showing multiple areas 401-404, each area corresponding to a separate layout pattern for the deep N-well. In general, the layout distribution of surface N-wells and surface P-type regions or P-wells on semiconductor device 400 is characterized by particular patterns. Semiconductor device 400 can be divided according to these particular patterns into multiple areas 401-404. Alternatively, semiconductor device 400 may have a single layout distribution of surface N-wells and surface P-type regions or P-wells.

15 Once the layout patterns of the surface N-wells and surface P-type regions or P-wells are recognized, a layout pattern for the deep N-well region can be selected for the particular area. The layout patterns for the deep N-well region include a diagonal sub-surface mesh structure (see Figure 5A), an axial sub-surface mesh structure (see Figure 7), a diagonal sub-surface strip structure (see Figure 6A and Figure 6B), and an axial sub-surface strip structure (see Figure 8A and Figure 8B). The factors evaluated in selecting a particular layout pattern for the deep N-well region include: providing a low resistance conductive path for routing the body-bias voltage and avoiding the isolation of the P-type region or P-well region 385 (Figures 3A and 3B) on which

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nFETS 380 are formed to allow the formation of conductive paths between P-well region 385 and a sub-surface layer (e.g., doped with P-type material) that is formed beneath the deep N-well region.

5 Moreover, the primary factors in determining which particular layout pattern for the deep N-well region to use are the type of layout pattern (e.g., horizontal strips or vertical strips) of surface N-wells (see Figures 3A and 3B)) and the separation length between adjacent surface N-wells (e.g., separation length d in Figure 3A, and separation length m in Figure 3B). Since each type of layout pattern of surface N-wells
10 (see Figures 3A and 3B) exhibits unique characteristics, a layout pattern for the deep N-well region is selected that is appropriate for those characteristics exhibited by the layout pattern of the surface N-wells. Within each area 401-404, adjustments to the layout pattern of the deep N-well can be made to overcome any violations of the layout design rules and to improve the factors described above.

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Figure 5A illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a diagonal sub-surface mesh structure 500 in accordance with an embodiment of the present invention. Rather than having a continuous planar layer for the deep N-well, multiple diagonal deep N-well (DDNW) regions are patterned
20 according to a layout pattern. As depicted in Figure 5A, each diagonal deep N-well region 510A-510E and 512A-512D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Diagonal deep N-well regions 510A-510E are formed in a first parallel orientation

while diagonal deep N-well regions 512A-512D are formed in a second parallel orientation. The first parallel orientation and the second parallel orientation are orthogonal to each other and are diagonal (or slanted) with respect to N-well regions of Figures 3A and 3B. In an embodiment, the first parallel orientation and N-well

regions of Figures 3A and 3B form an angle that is approximately 45 degrees.

Additionally, in an embodiment, the second parallel orientation and N-well regions of Figures 3A and 3B form an angle that is approximately 45 degrees. Thus, diagonal

deep N-well regions 510A-510E and 512A-512D form a diagonal sub-surface mesh structure 500 for routing the body-bias voltage V_{nw} to the N-well regions so that pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between N-well regions and diagonal sub-surface mesh structure 500 to provide a plurality of sub-surface conductive paths between N-well regions without isolating the P-well region located between N-wells. That is, diagonal sub-surface mesh structure 500 contacts N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

The orientation of diagonal sub-surface mesh structure 500 is diagonal with respect to the orientation of N-well regions of Figures 3A and 3B. In an embodiment,

diagonal sub-surface mesh structure 500 is rotated approximately 45 degrees with respect to N-well regions of Figures 3A and 3B. It should be understood that diagonal sub-surface mesh structure 500 can have other configurations. For example, gaps 540A and 540B between adjacent diagonal deep N-well regions can vary in size.

5 Moreover, the ratio of diagonal deep N-well regions to gap area 430 can vary.

Additionally, diagonal sub-surface mesh structure 500 enables nFETS (n-type MOSFETS) 380 (Figures 3A and 3B) to be body-biased in any manner by preventing isolation of a P-type region or P-well region 385 (Figure 3A and 3B) on which nFETS
10 380 are formed. Gap area 530 between diagonal deep N-well regions 510A-510E and 512A-512D prevents isolation of P-well region 385 and enables a conductive path between P-well region 385 and a sub-surface layer that is beneath diagonal deep N-well regions 510A-510E and 512A-512D. In an embodiment, the area of diagonal sub-surface mesh structure 500 is equally divided between diagonal deep N-well
15 regions (e.g., 510A-510E and 512A-512D) and gap area 530.

As discussed above, a contact for the body-bias voltage V_{nw} can be formed wherever there is free space, such as above N-well regions or above diagonal deep N-well regions 510A-510E and 512A-512D. Moreover, the location and size of the
20 diagonal sub-surface mesh structure 500 is based on the distribution of the N-wells and the P-type regions or P-wells, wherein the goal is to provide low resistance conductive paths for the body-bias voltage V_{nw} .

However, the size of diagonal sub-surface mesh structure 500 should avoid isolating P-type regions or P-wells 385 (Figures 3A and 3B) from sub-surface layers that are formed beneath diagonal deep N-well regions 510A-510E and 512A-512D.

Moreover, gap area 530 is sized so as to provide a low-resistance conductive path

5 between P-type regions or P-wells 385 and a sub-surface layer that is formed beneath diagonal deep N-well regions, wherein the greater the gap area 530 the lower the resistance of this conductive path. Additionally, lateral diffusion and lateral depletion

can further reduce gap area 530, potentially pinching-off this conductive path between

P-type regions or P-wells 385 and a sub-surface layer that is formed beneath diagonal

10 deep N-well regions. As a solution to this situation, gaps 540A and 540B between

adjacent diagonal deep N-well regions are made sufficiently wide to avoid pinching-off

this conductive path between P-type regions or P-wells 385 and a sub-surface layer

that is formed beneath diagonal deep N-well regions. Yet, as the number and size of

the diagonal deep N-well regions are increased, the resistance of the conductive path

15 for routing the body-bias voltage V_{nw} is decreased because there are larger and more

sub-surface conductive boundaries between N-well regions and diagonal deep N-well

regions. Hence, there is a trade-off between gap area 530 and diagonal deep N-well

regions in each design situation.

20 Figure 5B illustrates a top view of multiple N-wells (e.g., N-well_1 and N-well_2) and multiple diagonal deep N-well (DDNW) regions forming a diagonal sub-surface mesh structure in accordance with an embodiment of the present invention. Here, diagonal deep N-well regions 410A and 410B are orthogonal to diagonal deep N-well

regions 412A, 412B, and 412C. Thus, diagonal deep N-well regions 412A, 412B, 412C, 410A, and 410B form a diagonal sub-surface mesh structure 490 for routing the body-bias voltage V_{nw} to N-well_1 and N-well_2 so that pFETs 470 can be body-biased. In an embodiment, the area of diagonal sub-surface mesh structure 490 is
5 equally divided between diagonal deep N-well regions and gap area 430.

It should be understood that diagonal sub-surface mesh structure 490 can have other configurations. Gaps 440A and 440B between adjacent diagonal deep N-well regions can vary in size. Moreover, the ratio of diagonal deep N-well regions to gap
10 area 430 can vary. The regions 495 between diagonal deep N-well regions prevent isolation of P-well region 485 and enable a conductive path between P-well region 485 and a sub-surface layer that is beneath diagonal deep N-well regions 412A, 412B, 412C, 410A, and 410B.

15 A top view of multiple diagonal deep N-well (DDNW) regions forming a first diagonal sub-surface strip structure 600A in accordance with an embodiment of the present invention is illustrated in Figure 6A. In this layout pattern, each diagonal deep N-well region 610A-610D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Diagonal deep
20 N-well regions 610A-610D are formed in a first parallel orientation. The first parallel orientation is diagonal (or slanted) with respect to surface N-well regions (e.g., N-well_A, N-well_B, and N-well_C). In an embodiment, the first parallel orientation and the N-well regions form an angle that is approximately 45 degrees. In this case, the

combination of surface N-well regions (e.g., N-well_A, N-well_ B, and N-well_C) and the first diagonal sub-surface strip structure 600A forms a mesh-type arrangement for routing the body-bias voltage to surface N-well regions so that pFETs can be body-biased.

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As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between N-well regions and first diagonal sub-surface strip structure 600A to provide a plurality of sub-surface conductive paths between N-well regions without isolating P-well region located between N-wells. That is, first diagonal sub-surface strip structure 600A contacts N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

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As described above, the combination of surface N-well regions (e.g., N-well_A, N-well_ B, and N-well_C) and diagonal deep N-well regions 610A-610D, which form the first diagonal sub-surface strip structure 600A, facilitate the routing of the body-bias voltage V_{nw} to N-well regions so that pFETs can be body-biased. First diagonal sub-surface strip structure 600A can be utilized in areas of the semiconductor device that have a dense layout such as areas corresponding to an SRAM (static random access memory). It should be understood that first diagonal sub-surface strip structure 600A can have other configurations. Gap 640A between adjacent diagonal deep N-well

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regions can vary in size. Moreover, the ratio of diagonal deep N-well regions to gap area 630 can vary.

Figure 6B illustrates a top view of multiple diagonal deep N-well (DDNW)

5 regions forming a second diagonal sub-surface strip structure 600B in accordance with an embodiment of the present invention. In this layout pattern, each diagonal deep N-well region 612A-612D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Diagonal deep N-well regions 612A-612D are formed in a second parallel orientation. The
10 second parallel orientation is diagonal (or slanted) with respect to surface N-well regions (e.g., N-well_D, N-well_E, and N-well_F). In an embodiment, the second parallel orientation and N-well regions form an angle that is approximately 45 degrees. In this case, the combination of surface N-well regions (e.g., N-well_D, N-well_E, and N-well_F) and second diagonal sub-surface strip structure 600B forms a
15 mesh-type arrangement for routing the body-bias voltage to surface N-well regions so that pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well
20 regions. Hence, sub-surface conductive boundaries can be formed between N-well regions and second diagonal sub-surface strip structure 600B to provide a plurality of sub-surface conductive paths between N-well regions without isolating P-well region located between N-wells. That is, second diagonal sub-surface strip structure 600B

contacts N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

5 As described above, the combination of surface N-well regions (e.g., N-well_D, N-well_E, and N-well_F) and diagonal deep N-well regions 612A-612D, which form the second diagonal sub-surface strip structure 600B, facilitate routing of the body-bias voltage V_{nw} to N-well regions so that pFETs can be body-biased. Second diagonal sub-surface strip structure 600B can be utilized in areas of the semiconductor device
10 that have a dense layout such as areas corresponding to an SRAM (static random access memory). It should be understood that second diagonal sub-surface strip structure 600B can have other configurations. Gap 640B between adjacent diagonal deep N-well regions can vary in size. Moreover, the ratio of diagonal deep N-well regions to gap area 630 can vary.

15 Figure 7 illustrates a top view of multiple axial deep N-well (ADNW) regions forming an axial sub-surface mesh structure 700 in accordance with an embodiment of the present invention. As depicted in Figure 7, each axial deep N-well region 710A-710E and 712A-712D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Axial deep N-well
20 regions 710A-710E are formed in a first parallel orientation while diagonal deep N-well regions 712A-712D are formed in a second parallel orientation. The first parallel orientation and the second parallel orientation are orthogonal to each other and are

axially positioned with respect to N-well regions of Figures 3A and 3B. That is, the first parallel orientation and the second parallel orientation are oriented along an axis (e.g., y-axis or x-axis) in the same manner as N-well regions of Figures 3A and 3B. In an embodiment, the first parallel orientation is parallel to N-well regions of Figure 3A and is perpendicular to N-well regions of Figure 3B. Additionally, in an embodiment, the second parallel orientation is parallel to N-well regions of Figure 3B and is perpendicular to N-well regions of Figure 3A. Thus, axial deep N-well regions 710A-710E and 712A-712D form an axial sub-surface mesh structure 700 for routing the body-bias voltage V_{nw} to N-well regions so that pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between N-well regions and axial sub-surface mesh structure 700 to provide a plurality of sub-surface conductive paths between N-well regions without isolating P-well region located between N-wells. That is, axial sub-surface mesh structure 700 contacts N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

It should be understood that axial sub-surface mesh structure 700 can have other configurations. For example, gaps 740A and 740B between adjacent axial deep N-well regions can vary in size. Moreover, the ratio of axial deep N-well regions to gap area 730 can vary.

Additionally, axial sub-surface mesh structure 700 enables nFETS (n-type MOSFETS) 380 (Figures 3A and 3B) to be body-biased in any manner by preventing isolation of a P-type region or P-well region 385 (Figure 3A and 3B) on which nFETS 380 are formed. Gap area 730 between axial deep N-well regions 710A-710E and 712A-712D prevents isolation of P-well region 385 and enables a conductive path between P-well region 385 and a sub-surface layer that is beneath axial deep N-well regions 710A-710E and 712A-712D. In an embodiment, the area of axial sub-surface mesh structure 700 is equally divided between axial deep N-well regions (e.g., 710A-710E and 712A-712D) and gap area 730.

As discussed above, a contact for the body-bias voltage V_{nw} can be formed wherever there is free space, such as above N-well regions or above axial deep N-well regions 710A-710E and 712A-712D. Moreover, the location and size of axial sub-surface mesh structure 700 is based on the distribution of N-wells and P-type regions or P-wells, wherein the goal is to provide low resistance conductive paths for the body-bias voltage V_{nw} .

As described above, the size of axial sub-surface mesh structure 700 should avoid isolating P-type regions or P-wells 385 (Figures 3A and 3B) from sub-surface layers that are formed beneath axial deep N-well regions 710A-710E and 712A-712D. Moreover, gap area 730 is sized so as to provide a low-resistance conductive path between P-type regions or P-wells 385 and a sub-surface layer that is formed beneath

axial deep N-well regions, wherein the greater the gap area 730 the lower the resistance of this conductive path. Additionally, lateral diffusion and lateral depletion can further reduce gap area 730, potentially pinching-off this conductive path between P-type regions or P-wells 385 and a sub-surface layer that is formed beneath axial deep N-well regions. As a solution to this situation, gaps 740A and 740B between adjacent axial deep N-well regions are made sufficiently wide to avoid pinching-off this conductive path between P-type regions or P-wells 385 and a sub-surface layer that is formed beneath axial deep N-well regions. Yet, as the number and size of the axial deep N-well regions are increased, the resistance of the conductive path for routing the body-bias voltage V_{nw} is decreased because there are larger and more sub-surface conductive boundaries between N-well regions and axial deep N-well regions. Hence, there is a trade-off between gap area 730 and axial deep N-well regions in each design situation.

Figure 8A illustrates a top view of multiple axial deep N-well (ADNW) regions forming a first axial sub-surface strip structure 800A in accordance with an embodiment of the present invention. In this layout pattern, each axial deep N-well region 810A-810D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Axial deep N-well regions 810A-810D are formed in a first parallel orientation. The first parallel orientation is parallel to surface N-well regions (e.g., N-well_G, N-well_H, and N-well_I). In this case, the combination of surface N-well regions (e.g., N-well_G, N-well_H, and N-well_I) and first axial sub-surface strip structure 800A forms a mesh-

type arrangement for routing the body-bias voltage to surface N-well regions so that pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between N-well regions and first axial sub-surface strip structure 800A to provide a plurality of sub-surface conductive paths between N-well regions without isolating P-well region located between N-wells. That is, first axial sub-surface strip structure 800A contacts N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

As described above, the combination of surface N-well regions (e.g., N-well_G, N-well_H, and N-well_I), and axial deep N-well regions 810A-810D, which form first axial sub-surface strip structure 800A, facilitate routing of the body-bias voltage V_{nw} to N-well regions so that pFETs can be body-biased. First axial sub-surface strip structure 800A can be utilized in areas of the semiconductor device that have a dense layout and are oriented according to N-well regions of Figure 3B. It should be understood that first axial sub-surface strip structure 800A can have other configurations. Gap 840A between adjacent axial deep N-well regions can vary in size. Moreover, the ratio of axial deep N-well regions to gap area 830 can vary.

Figure 8B illustrates a top view of multiple axial deep N-well (ADNW) regions forming a second axial sub-surface strip structure 800B in accordance with an embodiment of the present invention. In this layout pattern, each axial deep N-well region 812A-812D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. Axial deep N-well regions 812A-812D are formed in a second parallel orientation. The second parallel orientation is parallel to surface N-well regions (e.g., N-well_J, N-well_K, and N-well_L). In this case, the combination of surface N-well regions (e.g., N-well_J, N-well_K, and N-well_L) and second axial sub-surface strip structure 800B forms a mesh-type arrangement for routing the body-bias voltage to surface N-well regions so that pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between N-well regions and second axial sub-surface strip structure 800B to provide a plurality of sub-surface conductive paths between N-well regions without isolating P-well region located between N-wells. That is, second axial sub-surface strip structure 800B contacts N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

As described above, the combination of surface N-well regions (e.g., N-well_J, N-well_K, and N-well_L), and axial deep N-well regions 812A-812D, which form second axial sub-surface strip structure 800A, facilitates routing of the body-bias voltage V_{nw} to N-well regions so that pFETs can be body-biased. Second axial sub-surface strip structure 800B can be utilized in areas of the semiconductor device that have a dense layout and are oriented according to N-well regions of Figure 3A. It should be understood that second axial sub-surface strip structure 800B can have other configurations. Gap 840B between adjacent axial deep N-well regions can vary in size. Moreover, the ratio of axial deep N-well regions to gap area 830 can vary.

STRUCTURE FOR SPANNING GAP IN DEEP N-WELL STRUCTURE FOR ROUTING BODY-BIAS VOLTAGE

5 As noted above, the following description of the present invention is equally applicable to a p-type substrate and an N-well process, as well as to an n-type substrate and a P-well process.

 As described above, the deep N-well region can have many different layout
10 patterns for routing the body-bias voltage. Examples of these layout patterns include a diagonal sub-surface mesh structure (Figures 5A and 5B), an axial sub-surface mesh structure (Figure 7), a diagonal sub-surface strip structure (Figures 6A and 6B), and an axial sub-surface strip structure (Figures 8A and 8B).

15 When a deep N-well structure is utilized to route the body-bias voltage, there are occasions when the deep N-well structure may be interrupted or separated in multiple sections by an isolation structure. Ideally, the deep n-well structure should not contact or cross the isolation structure because short circuit conditions can be created. This isolation structure is used for nFETs and/or pFETs that form specialized circuits
20 (e.g., I/O circuits, analog circuits, etc.) requiring voltages that are different than the voltages provided to core region nFETs and pFETs. Typically, the isolation structure has a strip configuration of various lengths. It should be understood that the isolation

structure can also be a deep N-well structure having a voltage bias that is different than the voltage bias of another deep N-well structure.

For isolating nFETs, the isolation structure is comprised of a continuous (surface) N-well perimeter and a solid deep N-well plate structure, forming a p-type isolation tub. For isolating pFETs, the isolation structure is comprised of a separate (surface) N-well. Moreover, the isolation structure can be configured for isolating both nFETs and pFETs. In this case, one or more perimeter sides of the continuous (surface) N-well perimeter of the isolation structure can help form the isolated pFETs.

Although the discussion below will focus on deep N-well mesh structures (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B)), the discussion is equally applicable to other deep N-well structures utilized to route the body-bias voltage.

Figure 9A illustrates a top view of a semiconductor device 100, showing a first deep N-well mesh structure 10, a second deep N-well mesh structure 20, and an isolation structure 70 formed between deep N-well mesh structures 10 and 20 to create a gap between deep N-well mesh structures 10 and 20 in accordance with an embodiment of the present invention. As depicted in Figure 9A, isolation structure 70 created a gap 15 in a deep N-well mesh structure 50, wherein gap 15 separated deep N-well mesh structure 50 into first deep N-well mesh structure 10 and second deep N-well mesh structure 20. Here, deep N-well mesh structure 50 is a diagonal deep N-

well mesh structure. Deep N-well mesh structure 50 is comprised of a plurality of diagonal deep N-well regions 52.

Figure 9B illustrates a top view of a semiconductor device 100, showing a deep N-well mesh structure 50 and an isolation structure 70 that creates a gap 15 in deep N-well mesh structure 50 in accordance with an embodiment of the present invention. As depicted in Figure 9B, isolation structure 70 created a gap 15 in a deep N-well mesh structure 50, wherein gap 15 interrupts deep N-well mesh structure 50 rather than separating it. Isolation structure 70 is formed within the perimeter of deep N-well mesh structure 50. Here, deep N-well mesh structure 50 is a diagonal deep N-well mesh structure. Deep N-well mesh structure 50 is comprised of a plurality of diagonal deep N-well regions 52.

Referring to Figures 9A and 9B, isolation structure 70 includes an N-well perimeter 74 and a solid deep N-well plate structure 25 (see Figure 10), forming a p-type isolation tub 76. Isolation structure 70 is utilized to form specialized circuits (e.g., I/O circuits, analog circuits, etc.), as described above.

Gap 15 interrupts the routing of body-bias voltage. However, if the area of gap 15 is sufficiently large to negatively affect the electrical resistance property of deep N-well mesh structure 50, corrective action has to be taken to reduce the impact of gap 15 (due to isolation structure 70) on the electrical resistance property of deep N-well mesh structure 50. As will be described below, at least one metal structure 80 (see

Figures 11A and 11B) is formed across the isolation structure 70 to address the impact of gap 15 (due to the isolation structure 70) on the electrical resistance property of the deep N-well mesh structure 50. Metal structure 80 (see Figures 11A and 11B) is coupled to deep N-well mesh structure 50 with tap contacts on opposite sides of isolation structure 70.

Figure 10 illustrates a cross-sectional view of semiconductor device 100 of Figure 9A along line A-B in accordance with an embodiment of the present invention. Deep N-well mesh structure 50 (see Figure 9A) is formed below surface 90. As shown in Figure 10, isolation structure 70 includes an N-well perimeter 74 and a solid deep N-well plate structure 25, forming a p-type isolation tub 76. Gap 15 separates deep N-well mesh structure 50 (see Figure 9A) into first deep N-well mesh structure 10 and second deep N-well mesh structure 20. First deep N-well mesh structure 10 does not contact isolation structure 70. Additionally, second deep N-well mesh structure 20 does not contact isolation structure 70. The first and second deep N-well mesh structures 10 and 20 are comprised of a plurality of diagonal deep N-well regions 52.

It should be understood that regions 94 and 96 are utilized to form nFETs and pFETs described in Figures 1-8B.

Figure 11A illustrates a top view of semiconductor device 100 of Figure 9A, showing a metal structure 80 for spanning isolation structure 70 in accordance with an embodiment of the present invention. Similarly, Figure 11B illustrates a top view of

semiconductor device 100 of Figure 9B, showing a metal structure 80 for spanning isolation structure 70 in accordance with an embodiment of the present invention.

Referring to Figures 11A and 11B, at least one metal structure 80 is utilized to span isolation structure 70. Metal structure 80 carries electrical current across isolation structure 70. While in Figure 11A tap contact 81 couples metal structure 80 to first deep N-well mesh structure 10, tap contact 81 couples metal structure 80 to deep N-well mesh structure 50 in Figure 11B. Moreover, while in Figure 11A tap contact 82 couples metal structure 80 to second deep N-well mesh structure 20, tap contact 82 couples metal structure 80 to deep N-well mesh structure 50 in Figure 11B. In an embodiment, metal structure 80 has a metal wire shape. It should be understood that metal structure 80 can have other shapes. For example, the portion of metal structure 80 that overlaps deep N-well structure 10 (Figure 11A), 20 (Figure 11A), and 50 (Figure 11B) can have a T-shape. This enables the formation of additional tap contacts from metal structure 80 to deep N-well structure 10 (Figure 11A), 20 (Figure 11A), and 50 (Figure 11B). This provides lower resistance between metal structure 80 and deep N-well structure 10 (Figure 11A), 20 (Figure 11A), and 50 (Figure 11B).

Metal structure 80 can be comprised of a single metal layer. Alternatively, metal structure 80 can be comprised of a plurality of metal layers. Furthermore, the number of metal structures 80 needed is dependent on several factors. These factors include the sheet resistance of deep N-well mesh structure, the sheet resistance of metal structure 80, and the width 83 of isolation structure 70.

In an embodiment, a deep N-well plate 51 (Figure 11A and Figure 11B) can be formed beneath metal structure 80 where tap contacts 81 and 82 are located. The deep N-well plate 51 is a continuous sub-surface layer rather than a sub-surface patterned layer as described in Figures 1-11B with respect to deep N-well structures for routing body-bias voltage. Each deep N-well plate 51 is coupled to deep N-well structure 10 (Figure 11A), 20 (Figure 11A), and 50 (Figure 11B). Thus, lower resistance between metal structure 80 and deep N-well structure 10 (Figure 11A), 20 (Figure 11A), and 50 (Figure 11B) is achieved. In an embodiment, deep N-well plates 51 are diagonally oriented (or rotated with respect to the position shown in Figures 11A and 11B) to provide greater intersection between deep N-well structure and deep N-well plate 51.

The values provided henceforth to determine the benefits of using metal structure 80 are illustrative. The present invention is not limited to these values. The values may be different in other cases for numerous reasons (e.g., manufacturing process utilized, materials utilized, etc.). The sheet resistance of deep N-well region is approximately 1000 ohms per square. The sheet resistance of deep N-well mesh structure 50 is approximately 2000 ohms per square. The sheet resistance of a metal sheet is approximately 0.2 ohms per square. The goal is to supply sufficient metal structure(s) to improve the resistance property of deep N-well mesh structure 50 having gap 15.

In an embodiment, the width of metal structure 80 is approximately 1 μm (or 1 unit) wide, wherein μm represents micrometers. Moreover, a metal structure 80 is placed approximately every 1000 μm or (1000 units), wherein μm represents micrometers. Thus, the sheet resistance of metal structure 80 is approximately 200 ohms per square (0.2×1000), since metal structure 80 (of approximately 1 μm width) is placed approximately every 1000 μm . Since the sheet resistance of a metal sheet is approximately 1000 times lower (or better) than the sheet resistance of deep N-well mesh structure 50, metal structure(s) 80 have no more electrical resistance than the electrical resistance of the portion of deep N-well mesh structure 50 that could occupy the area of gap 15.

Moreover, since metal structure 80 is placed every 1000 μm , the capacitance of metal structure(s) 80 does not appreciably increase the capacitance of deep N-well mesh structure 50. Thus, metal wire to metal wire coupled noise on metal structure 80 does not significantly contribute to body-bias voltage noise (or substrate noise).

Alternatively, metal structure 80 can be replaced with structures comprised of polysilicon wiring, diffusion wiring, or silicide wiring. However, these alternative implementations are less beneficial than using metal structure 80. Higher sheet resistance and a larger number of these structures formed across the isolation structure characterize these alternative implementations.

The above discussion focused on deep N-well mesh structures (e.g., diagonal sub-surface mesh structure of Figures 5A and 5B). However, the above discussion is equally applicable to other deep N-well structures utilized to route the body-bias voltage.

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The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The
10 embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.